

Lateral Field Emission Diodes Using SIMOX Wafer

Jung-Hyeon Park, Hyung-Il Lee, Heung-Sik Tae, Jeung-Soo Huh, and Jung-Hee Lee

Abstract—Lateral field emission diodes were fabricated by using separation by implantation of oxygen (SIMOX) wafer and their current–voltage characteristics (I – V) were analyzed. Applying conventional photolithography and local oxidation of silicon (LOCOS) process, we fabricated single-crystalline lateral silicon field emitters with very sharp cathode and anode tips and very short cathode to anode spacing ranging from 0.3 to 0.8 μm as well. Two different types of tips, tapered and wedge-shaped emitters, were typically formed according to oxidation time. The turn-on voltages for both types of diodes were as low as 22 ~ 25 V and the emission currents were as high as 6 $\mu\text{A}/\text{tip}$ at voltages of 35 ~ 38 V. From the Fowler–Nordheim (FN) equation, field emitting area (A) and field enhancement factor (β) for both types of diodes were estimated to explain the low turn-on voltages and the high emission currents.

I. INTRODUCTION

RECENTLY, there has been enormous interest in vacuum field emitters because of their great tolerance to high-temperature and high-radiation environments [1]–[2]. The field emitters, which have been proposed and fabricated to date, are largely divided into two groups, vertical and lateral structures [3]. The vertical field emitter arrays (FEA's) were usually fabricated by the use of silicon or Spindt-type metal tip [1]. They have some advantages that the cathode and the gate electrode are easily formed on the substrate and high emission current can be produced due to high packing density [4], which make it easy to be applied to the flat panel display [5] by suspending a collector plate above the substrate [6]. However, the lateral FEA's have many advantages in high-speed and high-frequency applications, owing to a simple fabrication process, easy shaping of the electrodes, and possibly very precise control of the distances between electrodes by using fine lithography [7]–[8].

Since the first proposal by Shoulder [9], various types of lateral FEA's, which are usually fabricated by using refractory metals with small work function such as W and Mo, have been investigated by many other research groups. Kanemaru *et al.* [7] reported the tungsten field emission triode with turn-on voltage of 80 V, arranged laterally on a quartz glass substrate. Ora *et al.* [8] fabricated lateral tantalum multitip diodes with emitter to anode spacing ranging from 0.03 ~ 0.5 μm by using high-resolution electron beam lithography. Mei *et al.* [10] realized the on-chip vacuum microdiodes with both

tungsten and polysilicon cold cathodes using directional material sealing technique. The turn-on voltage and maximum current capability of the diodes were about 30 V and 200 μA , respectively. In the cases of using metal or polysilicon tip, however, it is very difficult to form a sharp tip necessary for the locally strong field generation without the help of fine electron beam lithography and the long term stability remains questionable.

To overcome problems mentioned above, we proposed and fabricated, for the first time, single-crystalline lateral silicon field emitter by choosing separation by implantation of oxygen (SIMOX) wafer as substrate, and by using local oxidation of silicon (LOCOS) process and conventional photolithography, which resulted in very sharp tip formation and very short cathode-to-anode spacing.

II. DEVICE FABRICATION

A process flow diagram for the fabrication of the diodes is shown in Fig. 1. A SIMOX wafer [(100) oriented, p-type] with 3700-Å thick buried silicon oxide layer and 1900-Å top silicon layer, was employed as an emitting material. After standard initial cleaning, the SIMOX wafer was implanted with phosphorus ($1 \times 10^{14} / \text{cm}^2$, 50 keV) and annealed for 30 min in N_2 ambient at 900 °C to convert p-type top silicon layer to n^+ -layer. This n^+ -layer might help ease electron emission by decreasing the work function. A 0.2- μm layer of LPCVD silicon nitride was then deposited and patterned as shown in Fig. 1(a).

The pattern of the cathode tip was designed to overlap the anode in order to achieve very short spacing between electrodes. The overlap lengths of the patterned silicon nitride ranged from 0.3 to 0.8 μm . During the LOCOS process for tip formation, the oxidation time was varied to optimize the sharpness of the cathode and the spacing between electrodes. To precisely control the shape of the tip, we divided the oxidation process into two steps. All wafers were first oxidized in steam at 1100 °C for 1 h to reduce the lateral oxidation time necessary for a rough tip formation and then reoxidized in dry oxygen ambient at 1100 °C for various time to exactly control the tip sharpness and the inter-electrode spacing. Two different types of tips were typically formed according to dry oxidation time as shown in Fig. 2. The wedge-shaped tip could be formed with a very small cathode-to-anode spacing when the dry oxidation time was sufficient enough to make the tip vertically sharp but not laterally. The reason why the wedge-shaped tip [Fig. 2(a)] is formed is that as the top silicon layer is oxidized, it becomes vertically very thin and undergoes a strong tensile stress from the surrounding oxide layer, and hence can be split into two parts. Further

Manuscript received February 28, 1996; September 20, 1996. The review of this paper was arranged by Editor J. A. Dayton, Jr.

J.-H. Park, H.-I. Lee, and H.-S. Tae are with the School of Electronic and Electrical Engineering, Kyungpook National University, Taegu 702–701, Korea.

J.-S. Huh and J.-H. Lee are with the Department of Metallurgical Engineering, Kyungpook National University, Taegu 702–701, Korea.

Publisher Item Identifier S 0018-9383(97)03754-4.

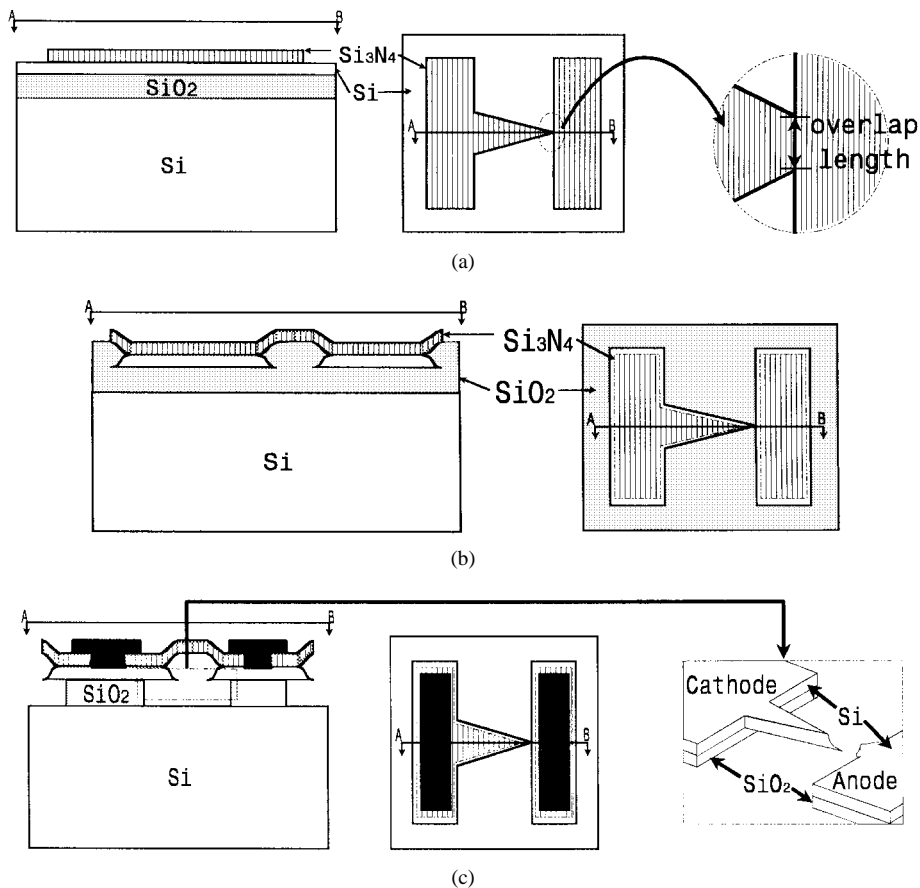


Fig. 1. The cross-sectional and top views of the fabrication steps: (a) cathode and anode definition, (b) LOCOS process for tip formation, and (c) contact open, metallization, and oxide etching (the figure in the inset shows the proposed tip shape after process; it is expected that the cathode tip is both vertically and laterally sharpened).

oxidation plays the role of sharpening the tip, especially in the lateral direction and results in forming a tapered tip [Fig. 2(b)] with a little increased cathode-to-anode spacing. Fig. 3 is the SEM photograph of the fabricated tip viewed at a tilted angle. The cathode-to-anode spacing ranges within 3000 ~4000 Å. It is clearly observed that the cathode tip is both vertically and laterally sharpened with the edge radius of the tip approximately equal to 100 Å.

III. RESULTS AND DISCUSSION

The bonded diodes were tested in a vacuum chamber with a pressure of less than 5×10^{-7} torr. No special cleaning or bake-out procedure was performed before electrical test. Fig. 4 shows current-voltage (I - V) characteristics for two different types of diodes having respective cathode-to-anode spacing of 4000 Å (wedge-shaped) and 6000 Å (tapered). For the wedge-shaped diode, the turn-on voltage is as low as 25 V and the operating voltage is 35 V, where the operating voltage is defined as the voltage required to obtain 6- μ A/tip. On the other hand, the tapered one exhibits a turn-on voltage of 22 V and an operating voltage of 38 V. The lower turn-on voltage of the tapered diode is attributed to a sharper tip and the lower operating voltage of the wedge-shaped diode is due to a smaller inter-electrode spacing and larger emitting area. Regardless of shapes, both types of diodes show the lowest

turn-on and operating voltages in comparison to the other lateral field emission diodes ever reported [7]–[10].

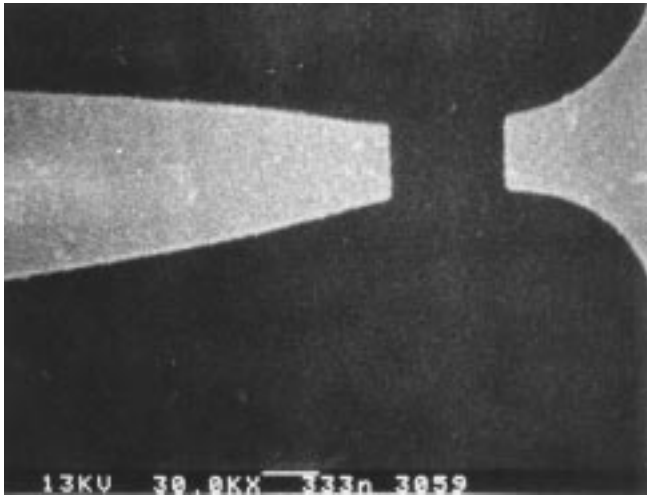
The basic field emission relationship between the emission current I in amperes and the applied voltage V in volts is obtained from the logarithmic Fowler–Nordheim (FN) equation given by

$$\log(I/V^2) = \log(a) + 0.434(-b/V) \quad (1)$$

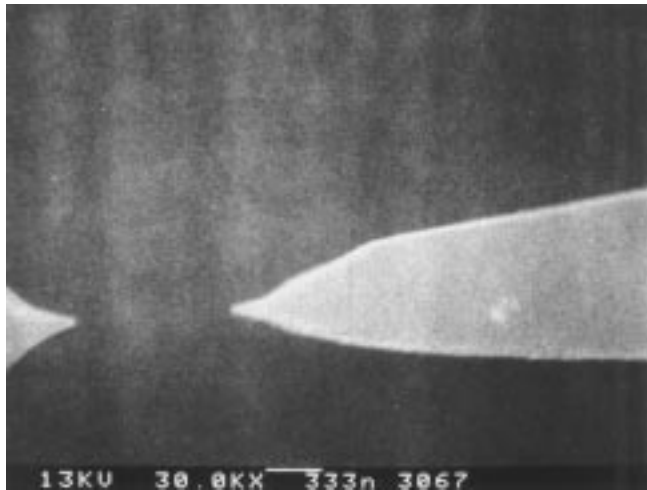
where $a \cong 1.5 \times 10^{-6} \frac{A}{\phi} \beta^2 \exp(10.4/\phi^{0.5})$, $b \cong 6.44 \times 10^7 \frac{\phi^{3/2}}{\beta}$, A is the emitting area in cm^2 , ϕ is the work function in eV, and β is the field enhancement factor in cm^{-1} dependent on the electrode configuration [11]. It is clear that an estimate of the apparent emitting area (A) and field enhancement factor (β) can be obtained from the slope of the FN plot and the intersection between the extrapolated line and the Y-axis.

Fig. 5 is a FN plots for the devices in Fig. 4. Good linearity of the measured curves, which are well fitted to simulation results [12], gives a confirmation of field emission. The estimated field emitting area of the wedge-shaped diode is larger than that of the tapered one, while the field enhancement factor is lower as shown in Fig. 5. This indicates that the field emitting area decreases and the field enhancement factor increases, as the dry oxidation time increases and consequently the tip is laterally sharpened.

We interpret the emitting areas shown in Fig. 5 as just a relative measure of tip sharpness and field enhancement



(a)



(b)

Fig. 2. SEM photographs of two different tips after thermal oxidation; (a) wedge-shaped tip (1100 °C, wet O₂ 1 h + 1100 °C, dry O₂ 2 h) and (b) tapered tip (1100 °C, wet O₂ 1 h + 1100 °C, dry O₂ 2 h 30 min.)

factor β between two different types of emitter shapes rather than explaining their exact physical dimensions. The emitting areas are very small compared to the values obtained in other results, typically $\sim 10^{-12} \text{cm}^2$, and the field enhancement factor β is one or two orders of magnitude higher. From the relationship between emitting area and the field enhancement factor ($A \propto 1/\beta^2$), we can expect that the emitting areas should be $\sim 10^{-16} \text{cm}^2$. However, very small values ($\sim 10^{-18} \sim 10^{-19} \text{cm}^2$) of emitting areas in the Fig. 5 cannot be explained clearly at this time.

As a possible explanation for this result, this very small emitting area is because both the cathode and anode are very sharp, which is different from other results, where only the cathode tip is sharp. This may cause unexpectedly high field enhancement and hence decrease the emitting area.

IV. CONCLUSION

We have fabricated, for the first time, single crystalline lateral silicon field emitters sharpened both vertically and

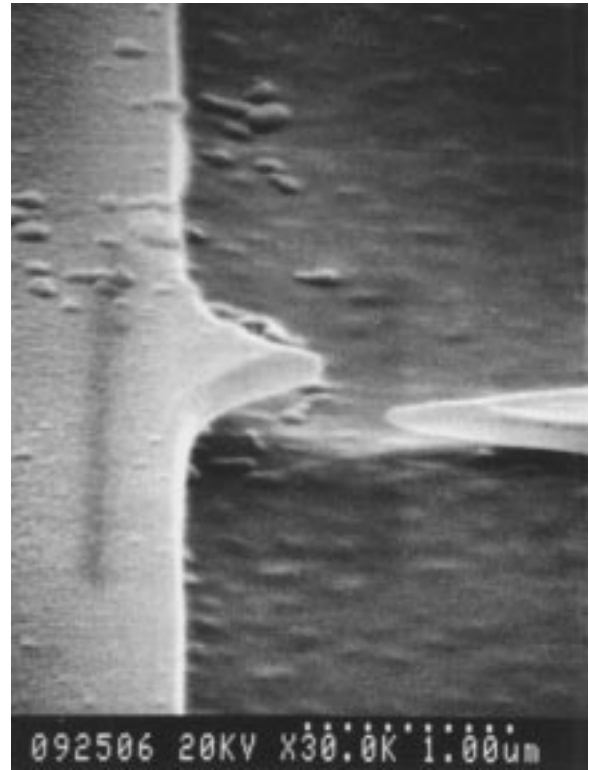


Fig. 3. The SEM photograph of the fabricated cathode tip by LOCOS.

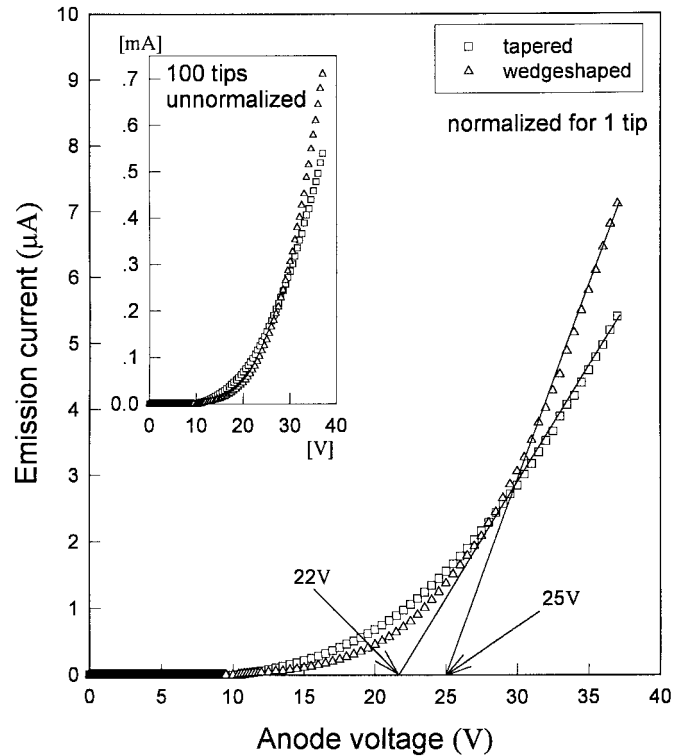


Fig. 4. $I-V$ characteristics of fabricated devices.

laterally by using a SIMOX wafer and applying conventional photolithography and the two-step LOCOS process. Two different types of emitters were formed according to the dry oxidation time. The turn-on voltages of the diodes ranged from 22 to 25 V, and emission current of 6 $\mu\text{A}/\text{tip}$ was obtained at

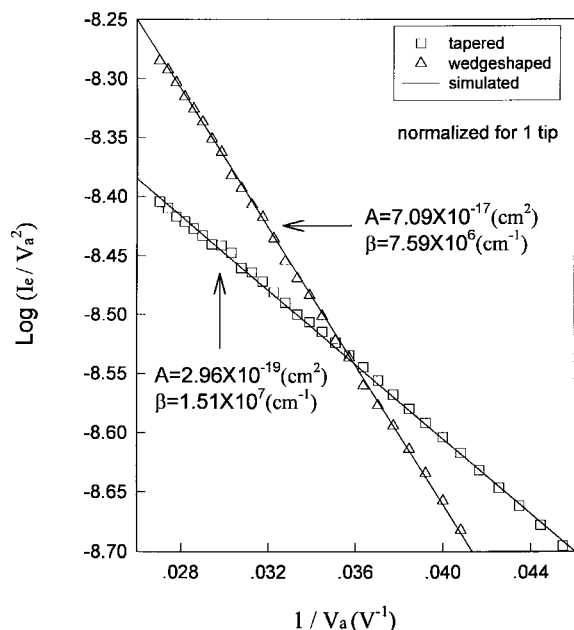


Fig. 5. Fowler-Nordheim (FN) characteristics of fabricated devices.

an anode bias of 35 ~ 38 V. From a FN plot, the field emitting area of the wedge type is larger than that of the tapered one, while the field enhancement factor is lowered.

REFERENCES

- [1] C. A. Spindt *et al.*, "Vacuum microelectronics," *Adv. Elec. Electron Phys.*, suppl. 4, p. 1, 1968.
- [2] I. Brodie *et al.*, "Acuum microelectronic devices," *Proc. IEEE*, 1994.
- [3] W. N. Carr *et al.*, "Comparison of vertical and lateral triode characteristics modeled performance," presented at *3rd Int. Conf. Vacuum Microelectron.*, Monterey, CA, 1990.
- [4] C. A. Spindt *et al.*, "Field-emitter arrays for vacuum microelectronics," *IEEE Trans. Electron Devices*, vol. 38, p. 2355, 1991.
- [5] R. Meyer, "Recent development on microtips display at LETI," presented at *4th Int. Conf. Vacuum Microelectron.*, Nagahama, Japan, 1991.
- [6] C. E. Holland *et al.*, "A study of field emission microtriodes," *IEEE Trans. Electron Devices*, vol. 38, pp. 2368-2372, 1991.
- [7] S. Kanemaru *et al.*, "Fabrication and characterization of lateral field-emitter triodes," *IEEE Trans. Electron Devices*, vol. 38, p. 2334, 1991.
- [8] J. A. Ora *et al.*, "Lateral field-emission devices with subtenth-micron emitter to anode spacing," *J. Vac. Sci. Technol. B*, vol. 11, no. 2, p. 464, 1993.
- [9] K. R. Shoulders, "Microelectronics using electron beam activated machining techniques," *Adv. Comput. F. L. Alt. Ed.*, vol. 2, p. 135, 1961.
- [10] Q. Mei *et al.*, "Planar-processed tungsten and polysilicon vacuum microelectronic devices with integral cavity sealing," *J. Vac. Sci. Technol. B*, vol. 11, no. 2, p. 493, 1993.
- [11] D. W. Branstion *et al.*, "Field emission from metal-coated silicon tips," *IEEE Trans. Electron Devices*, vol. 38, p. 2329, 1991.
- [12] H. Y. Ahn *et al.*, "Numerical analysis on field emission for the effects of the gate insulators," *J. Vac. Sci. Technol. B*, vol. 13, no. 2, p. 540, 1995.



Jung-Hyeon Park was born in Seoul, Korea, in 1971. He received the B.S. and M.S. degrees in electronic engineering from Kyung-Pook National University, Taegu, Korea, in 1994 and 1996, respectively.

Currently, he is with Hyundai Electronic Industry Company, Ltd., Ichun, Korea. His research interests are in high-speed semiconductor devices and ASIC design.



Hyung-II Lee was born in Taegu, Korea, on May 9, 1972. He received the B.S. degree in electronic engineering from Kyung-Pook National University, Taegu, in 1995. He is currently pursuing the M.S. degree at Kyung-Pook National University in the field of semiconductor microwave devices. His research involves developing a field emission device and its application.



Heung-Sik Tae was born in Seoul, Korea, in 1962. He received the B.S., M.S., and Ph.D. degrees in electrical engineering from Seoul National University, in 1986, 1988, and 1994, respectively. His doctoral research concerned plasma and low-temperature epitaxy technology.

Since 1995, he has been a Full-Time Instructor at the School of Electronic and Electrical Engineering, Kyung-Pook National University, Taegu, Korea. His current work involves ICP RIE and Gallium Nitride blue laser.



Jeung-Soo Huh was born in Taegu, Korea, in 1960. He received the B.S. and M.S. degrees in metallurgical engineering from Seoul National University, Seoul, Korea, and the Ph.D. degree in electronic materials from Massachusetts Institute of Technology, Cambridge, in 1983, 1985, and 1994, respectively. His doctoral research concerned Zinc Selenide Epitaxy using MOCVD.

From 1986 to 1987, he was a Research Assistant at Cornell University, Ithaca, NY, in the field of material engineering. From 1994 to 1995, he was with Korea Institute of Science and Technology (KIST), Seoul. Since 1995, he has been an Assistant Professor of metallurgical engineering at Kyung-Pook National University, Taegu. His current work involves the processing of electronic materials (MOCVD) and Gallium Nitride blue laser.



Jung-Hee Lee was born in Taegu, Korea, in 1957. He received the B.S. and M.S. degrees in electronic engineering from Kyung-Pook National University, Taegu, in 1979 and 1983, respectively, the M.S. degree in electrical and computer engineering from Florida Institute of Technology, Melbourne, in 1986, and the Ph.D. degree in electrical and computer engineering from North Carolina State University, Raleigh, in 1990. His doctoral research concerned Carrier collection and laser properties in monolayer-thick quantum well heterostructures.

From 1990 to 1993, he was with the Electronics and Telecommunication Research Institute (ETRI), Daechun, Korea, where he worked in the compound semiconductor research group. Since 1993, he has been Assistant Professor at the School of Electronic and Electrical Engineering, Kyung-Pook National University. His current work is focused on vacuum microelectronics, MMIC, and Gallium Nitride blue laser. He is the author or coauthor of 20 scientific papers.